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Research Article

Competitive Spike Pattern Detection for Neuromorphic systems

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ABSTRACT
Development of neuromorphic chips with biologically plausible learning mechanisms is vital for investigating brain-like learning processes. One such mechanism is Spike-timing dependent plasticity (STDP), but implementing its multi-bit circuitry requires significant silicon area. In a prior study, we introduced a hardware-friendly learning rule named adaptive STDP. Through experiments, we demonstrated its performance similarity to the ideal STDP rule in a basic biologically plausible spike pattern detection task involving a single neuron. Building upon this, our present study extends the adaptive STDP learning rule to encompass lateral inhibition, a prevalent motif in the brain. We apply it to a spike pattern detection model featuring multiple neurons that engage in competition to detect multiple patterns. Furthermore, we investigate the performance of the ideal STDP rule using 4-bit and 6-bit synapse resolution and present a comparative analysis of the results.

1. Introduction

Substantial global resources are dedicated to comprehending the brain's information processing and learning mechanisms. Development of neuromorphic chips with biologically plausible neuron and synapse circuits constitutes a fundamental component of this endeavor [1], [2]. Within the brain, neuronal cells engage in interaction at the microcircuit level via various (yet undiscovered) network motifs. To enhance our comprehension of brain microcircuits, it is essential to investigate these motifs through a bottom-up approach, constructing them at the level of neuronal cells and synapses. This process of exploration is facilitated by neuromorphic chips employing the "analysis by synthesis" methodology. By utilizing their neuron and synapse circuits, these chips can create scalable renditions of recognized network motifs, offering the potential to gain insights into network dynamics through real-time emulation. Furthermore, computational models of these mechanisms will contribute to the development of brain-like artificial intelligence, fostering potential applications in technologies that require ultra-low power consumption and online learning capabilities, such as Internet of Things (IoT) technology and Brain-Computer Interface (BCI) decoders.

In this study, our emphasis lies on the mixed-signal neuromorphic realization of a widely prevalent network motif, lateral inhibition with spike-timing dependent plasticity (STDP). We also provide post-silicon-validated circuit models for the same. Lateral inhibition is easily implemented in neuromorphic chips and many variants of STDP circuits have been proposed in the past. Nevertheless, the implementation of the ideal STDP rule often necessitates synapse circuits with remarkably high efficacy resolution, surpassing 10 bits. Such high resolution is attainable through pure analog circuits that store efficacy on a capacitor [3]. However, in these circuits capacitor leakage leads to loss of the learned efficacy over time, forgetting any learnt information. Bi-stable synapse circuits [4] address this leakage problem, but are limited to just two long-term stable states, offering a resolution of approximately 1.5 bits. This low resolution has a detrimental effect on the learning capability of the network causing it to deviate

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significantly from the performance of the ideal model. In mixed-signal circuits, efficacy is implemented using digital memories and digital-to-analog converters (DACs). The silicon area and energy requirements of DAC doubles with each additional bit of resolution. Consequently, the synapse resolution is constrained to about 4 to 6 bits in the majority of chips [1], [5]. Another approach involves the utilization of novel non-volatile memory devices such as ferro-electric field-effect transistors (FeFETs) and memristors for implementing synaptic efficacy [6], [7]. However, these devices are still in the research phase, and a consistent efficacy resolution exceeding 3 bits remains unattained. Furthermore, these devices come with their own implementation overheads. For instance, the FeFET device requires high-voltage programming pulses (> 2.5 V) to adjust the efficacy value.

Synapse resolution in the brain is a topic of debate, with some studies indicating bi-stable resolution while others suggesting the possibility of individual synapses having multi-bit resolution [8], [9]. Additionally, it has been observed that the STDP learning process is influenced not only by spike timing but also by the action of neurotransmitters. For instance, in the presence of dopamine, a neurotransmitter, the synapses are potentiated irrespective of the causal order of pre- and postsynaptic spikes [10].

Building upon this observation, a previous study introduced an adaptive STDP learning rule utilizing only 4-bit synaptic efficacy [11]. Its performance was demonstrated using a biologically plausible spike pattern detection model comprising a single neuron. Performance verification of the adaptive STDP rule encompassed numerical simulations as well as experimentation on a mixed-signal neuromorphic chip, showing similar results to the ideal STDP rule [11], [12]. The advantage of using the adaptive STDP rule lies in its relatively simpler circuitry compared to the circuit required for implementing the ideal STDP rule in a mixed-signal setup, which involves DACs and digital memory.

In this study, we apply the adaptive STDP rule to a more realistic biologically plausible network encompassing multiple neurons engaged in lateral inhibition. The input spike train model and the network motif were previously described in study that employed the ideal STDP rule with high-resolution synapses [13]. In this study, the same input and network motif are used but we employ the adaptive STDP rule with 4-bit synapses. We then compare its performance with the ideal STDP rule, which is constrained to 4-bit and 6-bit synapse resolutions suitable for implementation in neuromorphic hardware. All three STDP rules are of the additive type, with a bounded range, and consider only nearest neighbor spike pairs when calculating changes in synaptic efficacy.

The subsequent sections of this manuscript are structured as follows. Section 2 outlines the network model, providing details of the input spike trains, neuron, synapse, and the learning rules. Section 3 presents the obtained results, and the concluding section engages in a discussion of these findings and explores potential avenues for future research.

2. Network Model

The target network consists of nine neurons that inhibit each other in an all to all fashion. Each neuron receives stochastic input spikes through 2048 excitatory synapses. Within these stochastic spike trains, three distinct spike patterns are randomly embedded (as depicted in Fig. 1), with the network's objective being the recognition of these patterns. The embedded spike patterns are exclusively characterized by spike timings, emulating the temporal neural code observed across various brain regions. The input spike trains mirror those employed in the reference study [13], adhering solely to the statistical properties typically assumed in neuroscience. The spike train generation procedure is described next.

2.1. *Input Spike Train Model*

For each afferent (total of 2048 afferents), input spike trains were generated using an inhomogeneous Poisson process, where the instantaneous firing rate ranged from 0 to 90 Hz. The minimal interval for the frequency transition from 0 to 90 Hz was 50 ms. Each afferent spiked at least once in 50 ms establishing an average

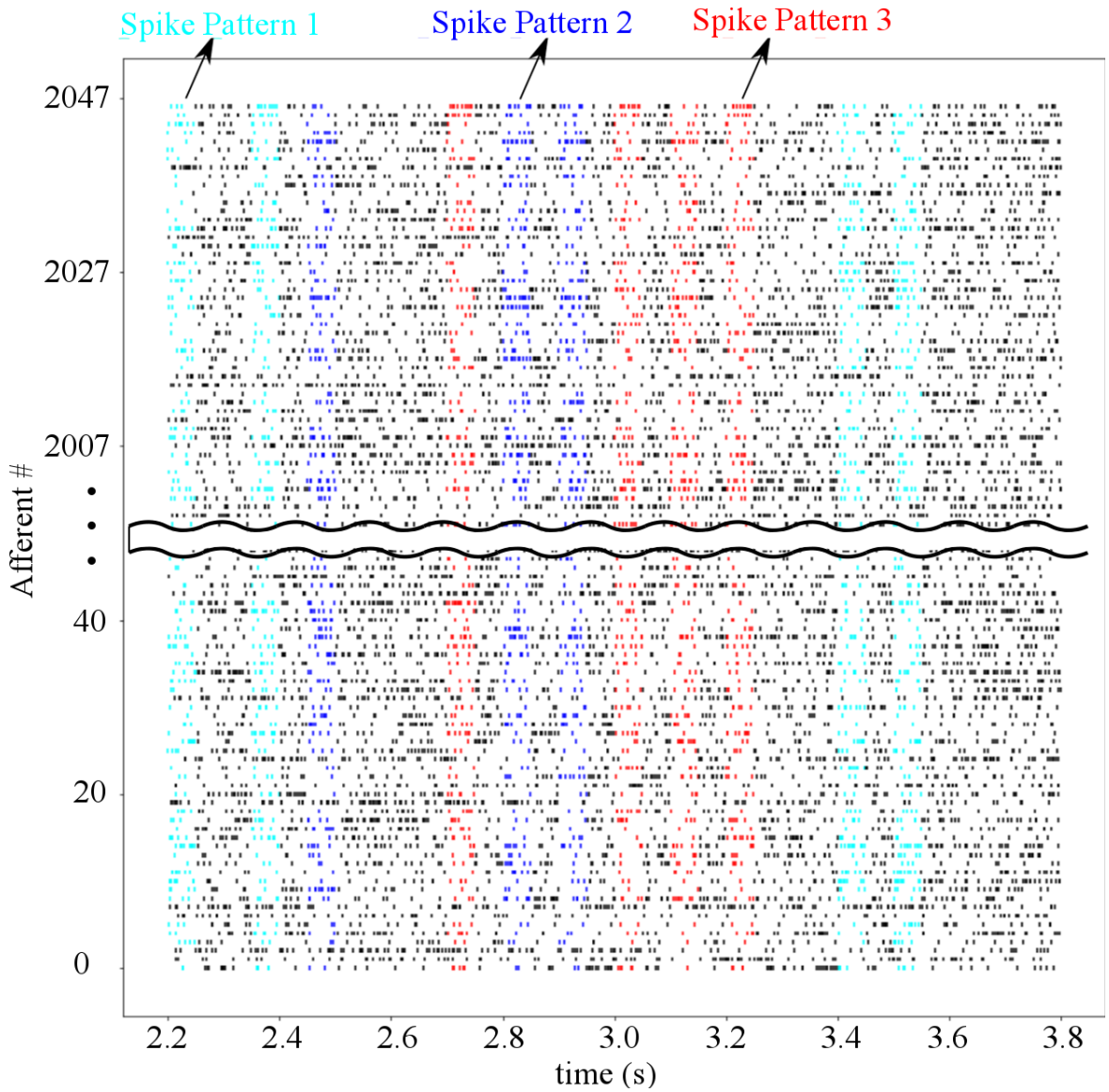

Fig. 1: The raster plot illustrates the input spike trains, featuring three embedded spike patterns distinguished by distinct colors. Each pattern is encoded by 1024 out of 2048 afferents. The spike trains exhibit jitter in spike timing within the patterns, with a standard deviation of 1 ms, alongside supplementary stochastic spikes at a frequency of 10 Hz. The afferents, on average, maintain a spiking frequency of 64 Hz. These spike patterns are temporally coded, specifically characterized by the spike timing of the afferents, while the spiking rate remains consistent both within and outside the patterns.

frequency of 54 Hz for each spike train. After generating stochastic spike train spanning 225 s, three segments, each lasting 50 ms and representing spike patterns to be embedded, were randomly selected from it. This ensures that the embedded spike patterns share similar characteristics with the stochastic Poisson spikes. The patter appearance frequency was set at 11.1 % for each pattern. Subsequently, the spike train was partitioned into 50 ms long sections, and a specific number of these sections, determined randomly based on the pattern appearance frequency, were replaced by the spike patterns to be embedded. This replacement was carried out sequentially, with pattern 1 being embedded first, followed by patterns 2 and 3. In other words, the three spike patterns collectively occupied one-third of the total simulation time. Additionally, a Gaussian jitter with a mean of zero and a standard deviation of 1ms is introduced in the spike patterns during the copy-paste process. This copy-and-replace process is exclusively administered to half of the randomly selected afferents

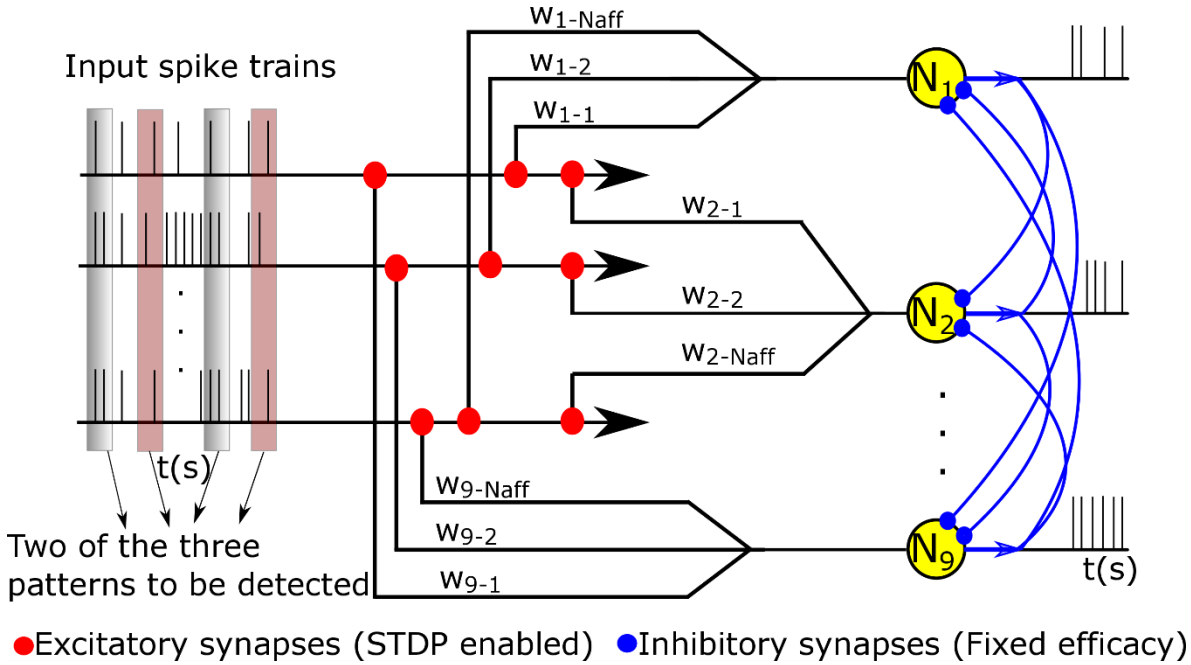

Fig. 2: Network model comprising nine LIF neurons (N1-N9) that laterally inhibit each other (blue connections). The neurons are simulated by 2048 synapses that receive input spike trains. The excitatory synapses are equipped with STDP and have efficacies bounded between 0 and 1. In contrast, the inhibitory synapses do not possess learning capability, and their efficacies remain constant.

(1024 out of 2048), while the remaining afferents solely encode stochastic spikes. Consecutive 50 ms sections were avoided in this copy-and-paste process. Both inside and outside the 50 ms long spike patterns, the population average spiking rate remains consistent, and the patterns are exclusively defined by the precise spike timing of the afferents. Subsequently, to further increase the difficulty of pattern detection, 10 Hz spontaneous spikes were incorporated into all the spike trains. This elevated the average firing rate to approximately 64 Hz across the afferent population.

2.2. *Neuron Model*

The network consists of nine leaky integrate-and-fire (LIF) neurons, each of which receive spike inputs through 2048 excitatory synapses as illustrated in Fig. 2. Similar to the reference study [13], we employ Gerstner's Spike response model (SRM) to model the neurons [14]. Whenever a presynaptic spike occurs at time t_j, an excitatory postsynaptic potential (EPSP) is added to the neuron's membrane potential. This EPSP kernel is described by

$$\varepsilon(t-t_j) = K \cdot \left(\exp\left(-\frac{t-t_j}{\tau_m}\right) - \exp\left(-\frac{t-t_j}{\tau_s}\right)\right) \cdot u(t-t_j), \quad (1)$$

where τ_m and τ_s are the membrane and synapse time constants, their values are 10 ms and 2.5 ms, respectively. The function u corresponds to the Heaviside step function. K is an arbitrary constant chosen so that the maximum amplitude of the EPSP kernel is 1. When the membrane potential exceeds a predetermined threshold (T), the neuron generates a spike. For every postsynaptic spike at time t_i, the spike profile and the after-hyperpolarization is described by

$$\eta(t-t_i) = T \cdot \left(K1 \cdot \exp\left(-\frac{t-t_i}{\tau_m}\right) - K2 \cdot \left\{\exp\left(-\frac{t-t_i}{\tau_m}\right) - \exp\left(-\frac{t-t_i}{\tau_s}\right)\right\}\right) \cdot u(t-t_j), \quad (2)$$

where constants K1=2 and K2=4 set the amplitude of the spike and the after-hyperpolarization, respectively. In addition, for every postsynaptic spike, the spiking neuron inhibits other neurons through inhibitory synapses adding an inhibitory postsynaptic potential (IPSP) to their membrane potential. This IPSP kernel is modelled using the EPSP kernel with a scaling factor of $\alpha = 0.25$ For a postsynaptic spike occurring at time t_k, it is described by

$$\mu(t-t_k) = -\alpha \cdot T \cdot (\epsilon(t-t_k)). \quad (3)$$

Combining the three kernels, the membrane potential of the neuron at any time instant is given by

$$v = \eta(t-t_i) + \sum_{j/t_j>t_i} w_j \cdot \varepsilon(t-t_j) + \sum_{j/t_k>t_i} \mu(t-t_k), \quad (4)$$

where w_j represents the synaptic efficacies of the excitatory synapses, which are constrained between the minimum value of 0 and the maximum value of 1. All three kernels are rounded off to zero when $t - t_{i,j,k}$

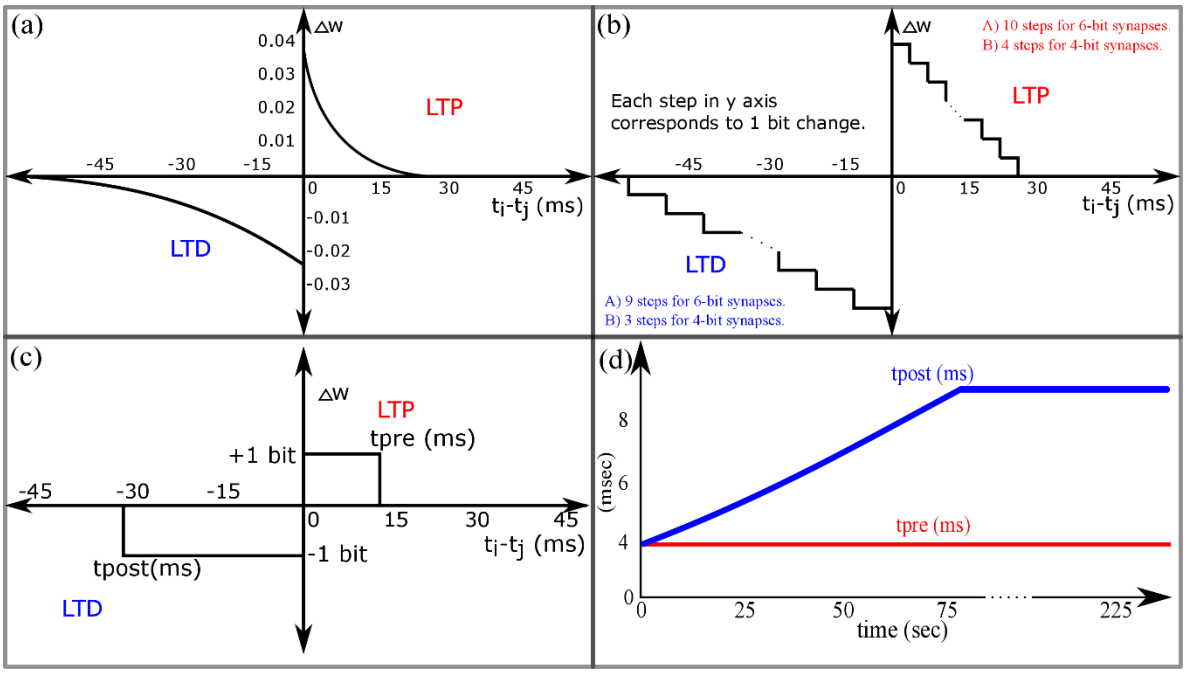

Fig. 3: STDP learning functions. (a) Ideal STDP rule that necessitates high-resolution synapses. (b) STDP rule constrained by synapse bit resolution. (c) Rectangular STDP rule. (d) Adaptive STDP rule: In the rectangular STDP rule, t_{post} is increased to higher values during learning while t_{pre} remains constant.

exceeds $7\tau_m$. Additionally, for every postsynaptic spike, the spiking neuron's EPSP and IPSP kernels are flushed.

The initial synaptic efficacies of excitatory synapses are randomly set and are subsequently modified while learning. The input spike trains containing the embedded spike patterns as described in Sec. 2.1 activate the excitatory synapses and cause the neurons to spike. The randomly assigned initial efficacy values initially determine the spiking frequency of neurons. Over time, with successive appearances of spike patterns, the learning rule modifies the synaptic efficacies and directs the neurons to spike in the presence of these patterns [11]. The introduction of lateral inhibitory synaptic connections induces competition among neurons, reducing the probability of multiple neurons spiking simultaneously within the same spike pattern. Consequently, this lateral inhibition enhances the likelihood that different neurons will learn distinct patterns or different segments within the 50 ms long pattern. The inhibitory synapses do not have learning capability and their efficacy remains constant.

2.3. *STDP-based Learning Rules*

2.3.1 4-bit and 6-bit STDP rule

The ideal STDP rule adjusts synaptic efficacy according to the spike interval between pre- and postsynaptic neurons, with the modification exhibiting an exponential dependence on the interval, as depicted in Fig. 3(a) [13]. This is mathematically expressed as:

$$\Delta w_j = \begin{cases} a^+ \cdot \exp\left(\frac{t_j - t_i}{\tau^+}\right) & \text{if } t_j \le t_i \quad (LTP), \\ a^- \cdot \exp\left(-\frac{t_j - t_i}{\tau^-}\right) & \text{if } t_j > t_i \quad (LTD), \end{cases} \tag{5}$$

where t_i (t_j) denotes the timing of the postsynaptic (presynaptic) spike, $\tau^-(\tau^+)$ denotes the time constant of the decaying exponential controlling depression (potentiation) of synapses is, and the learning rate a^- (a^+) controls the maximum change in the value of synaptic efficacy at any instant during depression (potentiation). In the reference study [13], following values were used $a^+ = 0.03125$, $a^- = 0.85 \cdot a^+$, $\tau^+ = 16.8$ ms, $\tau^- = 33.7$ ms. These values keep the function biased towards depression as $a^+\tau^+ < a^-\tau^-$. We use these parameters as reference to tune the values for 4-bit and 6-bit STDP rules.

In mixed-signal circuit implementation of STDP rule with DAC and digital memory, the resolution

of DAC is generally constrained to under 6 bits. Here we approximate the exponential traces of the learning function by a staircase-like traces as shown in Fig. 3(b). The synaptic efficacies for 4 (6)-bit synapses are quantized to 16 (64) different values and a single bit change corresponds to efficacy change by 0.667 (0.0159). The minimum possible change in the value of synaptic efficacy is 1 bit and the maximum possible change depends on the number of steps in the staircase-like function in Fig. 3(b). The number of steps for potentiation is kept higher than that for depression to keep a close approximation to the ideal learning function in Fig. 3(a). Best results were obtained with 4 (3) steps in the 4-bit case and 9 (8) steps in the 6-bit case for the potentiation (depression) function. The learning parameters $\tau+$ and $\tau-$ were the same as the reference values of 16.8 ms and 33.7 ms, respectively. In the case of 4-bit alone, the gap between the learning parameters $\tau+$ and $\tau-$ had to be further modified to 13.8 ms and 43.7 ms, respectively to bias the network parameters towards depression. With the ideal model values of 33.7 ms and 16.8 ms, learning did not occur.

2.3.2 4-bit Adaptive STDP rule

The adaptive STDP rule and its circuit implementation is described in detail in [11], [12]. It is illustrated in Fig. 3(c), Fig, 3(d) and is mathematically described as follows

$$\Delta w_j = \begin{cases} +1 \text{ bit}, \text{if } t_j \le t_i, t_i - t_j < t_{\text{pre}}, \text{and w} < w_{\max} \\ -1 \text{ bit}, \text{if } t_j > t_i, t_j - t_i < t_{\text{post}}, \text{ and w} > w_{\min} \end{cases}, (6)$$

where t_i (t_j) denotes postsynaptic (presynaptic) spike times, and $t_{\text{post}}(t_{\text{pre}})$ represents the maximum delay of the presynaptic (postsynaptic) spike following the postsynaptic (presynaptic) spike that leads to depression depression, LTD (potentiation, LTP). Unlike the STDP rule in Fig. 3(a), Fig. 3(b), the update in efficacy at any time instant is restricted to 1-bit, which simplifies its circuit implementation significantly. The 4-bit efficacy saturates at its maximum value of $w_{\max} = 1$ and minimum value of $w_{\min} = 0$. The learning parameter t_{pre} is set to 4.6 ms and t_{post} is increased gradually during learning from 5 ms to higher values saturating at 9.8 ms as shown in Fig. 3(d).

3. Results

Here we present the simulation results that quantify the performance of the network in Fig. 2. utilizing the three learning rules. A total of 100 simulation runs were conducted using (100 different) inputs spike trains generated according to the procedure detailed in Sec. 2.1. A run was deemed to be successful when all three spike patterns were detected with a hit rate surpassing 95 % and false alarms occurring at a rate below 1 Hz during the final 150 s of the run (one-third of the total run time), similar to the success criterion in the reference study [13]. The success rate was calculated using all runs that met the hit rate and false alarm criterion.

The performance with the three different learning rules are tabulated in Table 1. The best performance is observed with 6-bit STDP rule where all three patterns are detected by atleast one of the nine neurons in all the runs. The adaptive STDP rule and the 4-bit STDP rule have similar performance. The superimposed membrane potentials of nine neurons during a successful run employing the adaptive STDP rule are shown in Fig.4(a), while Fig.4(b) illustrates the same during the final second of the run. The three 50-ms long color-shaded segments indicate the location of three spike patterns within which the neurons learn to spike.

4. Discussion

This study investigated the implementation of the motif of lateral inhibition in a neuromorphic system incorporating STDP-based learning rules. Previous studies have demonstrated the presence of this motif in

Table 1
Summary of simulation results. The number of steps in the learning function or the maximum allowable change in efficacy is represented by Δw_{max}.

Learning Rule	Synapse Resolution	Parameters	Success Rate
Adaptive STDP	4-bit	t_{pre}= 4.6 ms, $t_{\text{post\_max}}$=9.8 ms, Δw_{min}=Δw_{max} =1/15, T=370	93 %
STDP	6-bit	τ^+= 16.8 ms, τ^-=33.7 ms, Δw_{min}=1/63, $\Delta w_{max} = 10 * \Delta w_{min}$, T=500	100 %
	4-bit	τ^+= 13.8 ms, τ^-=43.7 ms, Δw_{min}=1/15, $\Delta w_{max} = 4 * \Delta w_{min}$, T=500	88 %

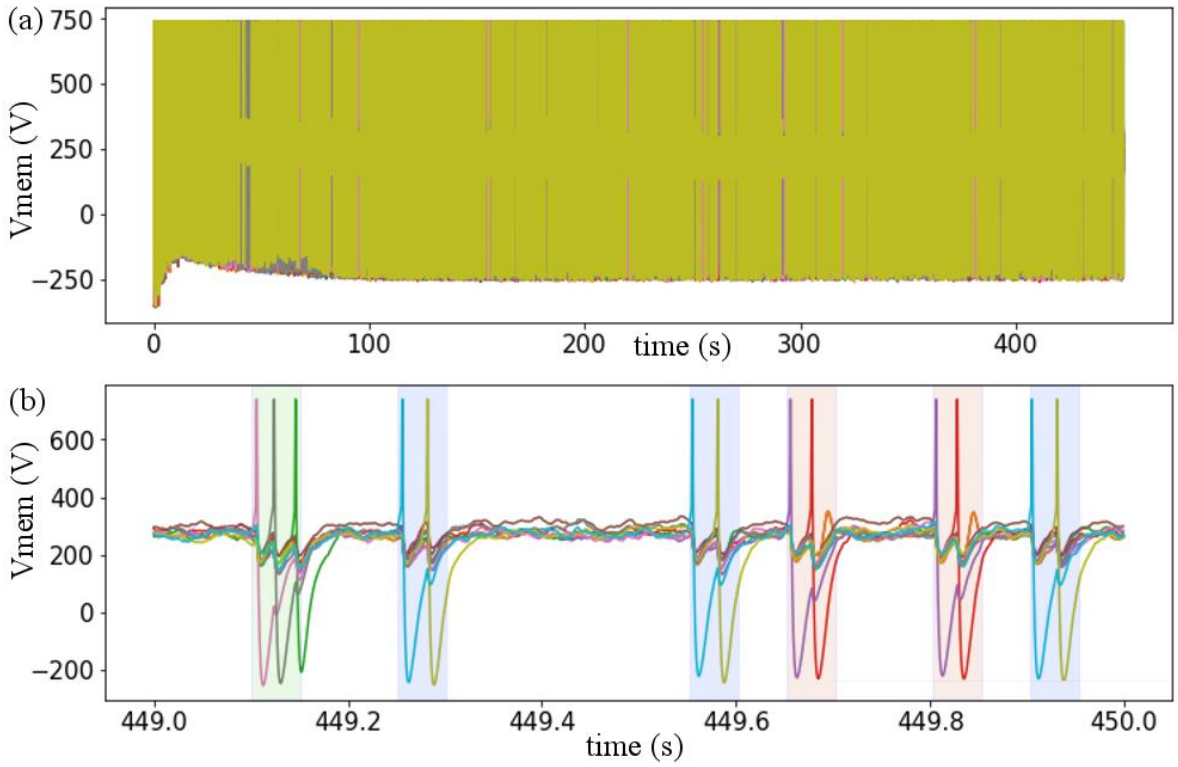

Fig. 4: Superimposed membrane potentials of nine neurons (a) across the complete run duration; (b) during the final second of the run. During the initial phase of the run, the neurons spike randomly and in time they learn to spike within the patterns. Three distinct colour shaded segments represent the three spike patterns. Two neurons stop spiking and the remaining seven neurons learn different segments of the three embedded 50-ms long spike patterns.

various brain regions and showed its ability to classify spike patterns [15], [16]. In our study, we specifically examined the performance of this motif by constraining the resolution of synaptic efficacy to be equal to 4 and 6 bits. We conducted a comparative analysis, evaluating the adaptive STDP rule employing 4-bit synapses against both 4-bit and 6-bit STDP rules, using a biologically plausible spike pattern classification task. Our findings indicate that all three rules achieved reliable pattern classification performance, with the 6-bit ideal STDP rule demonstrating the highest performance.

Although the 6-bit ideal STDP rule demonstrates better performance, its implementation in mixed-signal neuromorphic chips has a considerable overhead. Specifically, compared to a 4-bit synapse circuit, a 6-bit synapse requires approximately four times more silicon area and consumes more power. Additionally, the 4-bit and 6-bit STDP models require implementation of the staircase-like function shown in Fig. 3(b). This requires additional circuit components such as adders, subtractors, and lookup tables. In contrast, the adaptive STDP rule does not require these extra components. Since the adaptive STDP rule restricts efficacy change to one bit at a time, an up-down counter circuit is sufficient for updating the efficacy values.

The advantage of using adaptive STDP rule is its simplified circuitry, which consumes less silicon area and power compared to any ideal STDP circuit of similar bit resolution. A circuit to implement adaptive STDP is described in [12], where it was shown that its performance on a mixed-signal chip is similar to the ideal STDP model. This study extends this validation by demonstrating its scalability to larger networks capable of detecting multiple patterns. This scalability suggests that the adaptive STDP rule is well-suited for large-scale implementation and exploration of lateral inhibitory networks on neuromorphic chips.

The input spike train model was chosen due to its biological plausibility, and all network parameters were manually tuned to achieve optimal performance. It was observed that the learning parameters for the adaptive STDP rule varied depending on the chosen neuron model. In [11], a compartmental neuron model with a qualitatively modeled soma compartment was employed,

and the learning parameters t_{pre} and $t_{\text{post\_max}}$ around 10 ms and 35 ms, respectively, yielded the best performance. In contrast, in this study using a single compartment LIF neuron model, the best performance was achieved with t_{pre} and $t_{\text{post\_max}}$ approximately at 4.6 ms and 9.8 ms, respectively. The exploration of parameter dependence on the chosen neuron model will be further investigated in future studies.

For the 6-bit STDP rule, the learning parameters $\tau+$ and $\tau-$, similar to those used in the high-resolution STDP rule [13] (Fig. 3(a)), performed well. However, in the 4-bit case, the values of $\tau+$ and $\tau-$ had to be adjusted from their reference values of 16.8 ms and 33.7 ms to 13.8 ms and 43.7 ms, respectively. Furthermore, in the 4-bit and 6-bit ideal STDP rules, the number of steps in the learning function, which control the maximum allowable change in synaptic efficacy at any given time, played a significant role in the network's performance. The number of steps for the 4-bit and 6-bit cases differed, and they were chosen through manual tuning using multiple combinations. It is possible that the performance of the network for the 4-bit case be further improved by selecting a better set of parameters and this should be explored in the future studies.

Compared to the reference study [13], which employed the high resolution ideal STDP rule, and our previous study, which utilized the unidirectional two-compartment neuron model with the 4-bit adaptive STDP rule [17], the results in this study demonstrate significant improvement. In both previous studies, only in about two-thirds of the runs (~65-70 out of 100) all three patterns were successfully detected. However, an issue was identified during the investigation, revealing a bug in the code responsible for generating the input spike trains. This bug led to the unintentional deletion of the embedded spike patterns (either one or two out of three) in the generated spike trains. Specifically, this occurred when, during the random copy-and-paste process of embedding the spike patterns, the first or second spike pattern was placed in the last 50-ms slot of the 225-s long spike train. As a consequence of the missing spike patterns in certain input spike trains, the overall performance was negatively affected

In this study, the network was confined to a single layer, and the neurons learned a short segment within the 50-ms long patterns (Fig. 4(b)). A multi-layered network could potentially detect patterns of longer duration. Also, in the adaptive STDP rule, only the parameter controlling depression, (t_{post}) was modified while learning. The parameter t_{pre}can also be modified while learning, and these adjustments could be contingent on the network's state rather than relying on preprogrammed external control. Like the learning rules in this study, most neuromorphic chips implementing STDP-based rules only consider nearest neighbor spike pairs to modify the efficacy values. However, many variations of the STDP rule with multi-spike interactions have been observed in the brain [18], [19]. It is crucial to develop implementations of these rules with minimal hardware requirements for the development of biologically plausible neuromorphic chips. These potential modifications will be investigated in future studies.

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Authors Introduction

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He obtained his B. Tech degree in electronics and instrumentation engineering from Pondicherry University, India, in 2012. Later, he pursued his PhD in electrical engineering, earning his degree in 2021 from the University of Tokyo, Tokyo, Japan, where he presently serves as a Project Researcher.

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